

**400G QSFP-DD 10KM
Multi-Transceiver**

SF517A-LC-10KM

Product Brochure

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Product Introduction :

SF517A-LC-10KM is a high-performance solution for 400GE links for up to 10 km/6 km over single mode fiber (SMF). It combines 8x 26.5625GBd PAM4 electrical lanes into 4x 53.125 GBd PAM4 optical channels in compliance with 100G Lambda MSA 400G-LR4-10 and IEEE 400GBASE-LR4-6. Superior performance and reliability is achieved through CIG's advanced transmitter and receiver design using cooled EA-DFB-LDs each at a CWDM 1.3 μm wavelength and 4x PIN PDs with Non_x0002_hermetic COB. The 4 optical transmit and receive lanes are WDM'ed on to a single fiber pair through an LC connector.



Key Features:

- 400G-LR4-10 / 400GBASE-LR4-6 compliant
 - 4x 53.125 GBd PAM4
- 400GAUI-8 compliant
 - 8x 26.5625 GBd PAM4
- QSFP-DD MSA compliant
- LC connector
- Compliant with CMIS 4.0
- EEPROM Rewritable
- Low Power Consumption
- Less than 10W in temperature range of 0 to 70°C

Absolute Maximum Ratings:

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	85	°C
Case Operating Temperature	Top	0	70	°C
Relative Humidity (non-condensation)	RH		85	%
Supply Voltage	Vcc	0	3.6	V
Receiver Damage Threshold, per Lane	PRdmg		+7.1	dBm

Recommended Operating Conditions:

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Top	0	70	°C
Relative Humidity(non-condensing)	RH	5	85	%
Power Supply Voltage	Vcc	3.135	3.465	V
Total Power Consumption	Pc	-	8	W
Instantaneous peak current	Icc_ip_4		3200	mA
Sustained peak current	Icc-sp_4		2640.3	mA
Supply Current	Icc-4		2551.8	mA

Parameter	Symbol	Min	Typical	Max	Unit
Data rate per lane	DR	-100ppm	26.5625	+100ppm	GBd
AC Common-mode output voltage (RMS)				17.5	mV
Differential peak-to-peak output voltage				900	mV
Near-end ESMW (Eye symmetry mask width)		0.265			UI
Near-end Eye height, differential		70			mV
Far-end ESMW (Eye symmetry mask width)		0.2			UI
Far-end Eye height, differential		30			mV
Far-end pre-cursor ISI ratio		-4.5		2.5	%
Differential termination mismatch				10	%
Transition time (20% to 80%)		9.5			ps
DC common mode voltage		-350		2850	mV

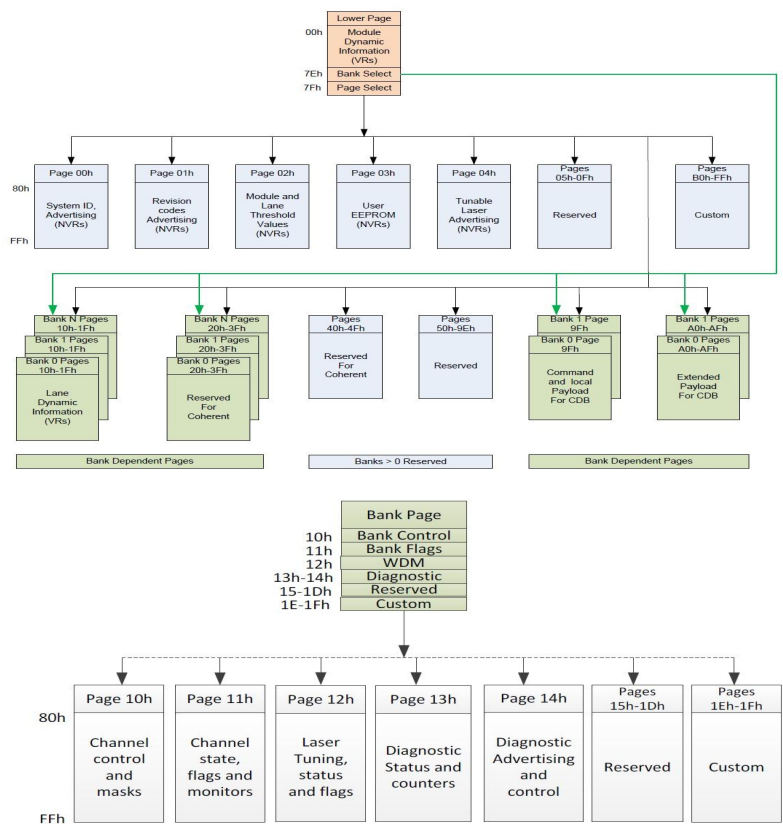
Optical Characteristics:

Parameter	Symbol	Min	Typical	Max	Unit
Channel data rate	fDC	106.25			Gbit/s
Signaling rate, each lane	fSG	53.125			GBd
Signal speed variation from nominal, each lane	Δf_{SG}	-100		+100	ppm
Side-mode suppression ratio	SMSR	30			dB
Average receive power, each lane		-2.7		5.1	dBm
Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			3.9	dB
Average optical output power of OFF Transmitter, each lane	Poff			17	ps
Transmitter transition time				25	%
Transmitter over/under-shoot		-30			dBm
Optical return loss tolerance				15.6	dB
Transmitter reflectance				-26	dB

Electrical Specification:

Parameters	Min	Typical	Max	Unit
Supply voltage	3.135	3.3	3.465	V
Supply Current			3.19	A
Input differential impedance	90	100	110	Ω
Differential data input swing			880	mVpp
Differential data output swing			900	mVpp
Bit Error Rate			2.4E-4	
Input Logic Level High	2		Vcc	V
Input Logic Level Low	0		0.8	V
Output Logic Level High	Vcc-0.5		Vcc	V
Output Logic Level Low	0		0.4	V

Management Interface:



Application Advertising:

Address (Dec)	Application		Value (Hex)	Description
	AppSel Code	Name		
85	NA	Module Type encoding	1	Optical Interfaces: MMF
86	0001b	HostInterfaceID	4B	HostInterfaceIDApp1:400GAUI-8 C2M
87		MediaInterfaceID	D	MediaInterfaceIDApp1:400GBASE-SR8
88		HostLaneCount&MediaLaneCount	11	LaneCountApp1: TX & RX 8 lanes
89		HostLaneAssignmentOptions	FF	Permissible first host lane number: lanes 1
01h:176		MediaLaneAssignmentOptions	FF	Permissible first media lane number: lanes 1
90	0010b	HostInterfaceID	11	HostInterfaceIDApp2:200GAUI-4 C2M
91		MediaInterfaceID	10	MediaInterfaceIDApp2:200GBASE-SR4
92		HostLaneCount&MediaLaneCount	88	LaneCountApp2:TX & RX 4 lanes
93		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1,5
01h:177		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1,5
94	0011b	HostInterfaceID	E	HostInterfaceIDApp3:100GAUI-2 C2M
95		MediaInterfaceID	0	MediaInterfaceIDApp3:100GBASE-SR2
96		HostLaneCount&MediaLaneCount	88	LaneCountApp3:TX & RX 2 lanes
97		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1,3,,5,7
01h:178		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1,3,,5,7
98	0100b	HostInterfaceID	51	HostInterfaceIDApp4: 50GAUI-1 C2M
99		MediaInterfaceID	12	MediaInterfaceIDApp4: 50GBASE-SR
100		HostLaneCount&MediaLaneCount	88	LaneCountApp4:TX & RX 1 lanes
101		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1, 2, 3, 4, 5, 6, 7, 8
01h:179		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1, 2, 3, 4, 5, 6, 7, 8
102	0101b	HostInterfaceID	4F	HostInterfaceIDApp5: 200GAUI-8 C2M
103		MediaInterfaceID	11	MediaInterfaceIDApp5:MSA Undefined(200G-SR8)
104		HostLaneCount&MediaLaneCount	44	LaneCountApp5:TX & RX 8 lanes
105		HostLaneAssignmentOptions	11	Permissible first host lane number: lane 1
01h:180		MediaLaneAssignmentOptions	11	Permissible first media lane number: lane 1

Application Selection and Instantiation:

The host can select Applications by programming the AppSel value in Staged Set 0. AppSel=1 is the default Application populated in the Active Control Set at power-on or reset.

Note: that the channels of the module are independent and can be configured separately. (ie. up to eight 50GBASE-SR instances can be configured), however, it does not support different applications with different channels at the same time

QDMD-85SRC supports two methods of application selection and instantiation. The first method is implemented according to CMIS, and the second method is customized, which is simpler.

First method:

The applications switching configuration sequence is as follows: read Application Descriptor Registers and select the required Appsel. Write application configuration to DPConfigLane<i> in Stage Control Set 0, then write 1 to ApplyDPInitLane<i> to trigger Application Instantiation.

The Active Set can be read from page11h.

For example, select AppDescriptor3:

Step 1: Write 0x30 in Page10h Byte145~Byte152(8 bytes)—Set AppselCode3

Step 2: Write 0x00 in Page10h Byte143—Clear trigger register.

Step 3: Write 0xFF in Page10h Byte143—Set trigger register to run Application Instantiation.

Second method:

Set the value of Page10h Byte240. This is a private definition.

Code Value	Bit Pattern	Host Electrical Interface	Media Interface
0	00000000b	400GAUI-8 C2M	400GBASE-SR8
1	00000001b	200GAUI-8 C2M	200GBASE-SR8
2	00000010b	100GAUI-2 C2M	100GBASE-SR2
3	00000011b	50GAUI-1 C2M	50GBASE-SR
4	00000100b	200GAUI-4 C2M	200GBASE-SR4

TX & RX Squelch:

Default TX and RX auto-squelch is enabled. But TX and RX auto squelch disable, and force squelching function are not supported.

TX input equalization:

Default TX adaptive equalization is enabled. But TX adaptive equalization disable, and fixed equalization adjust function are not supported.

RX output Equalization:

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	Reserved	Reserved
11-15	1011b-1111b	Custom	Custom

RX output amplitude:

RX output amplitude follows CMIS Table 6-8, Rx output amplitude is the difference peak-topeak EYE high when Rx output equalization is set to 0dB. The default value of output amplitude is set to 2, with typical differential 600mVp-p.

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)
4-14	0100b-1110b	Reserved
15	1111b	Custom

Loopback capabilities:

Media side input loopback and Host side input loopback feature are supported; loopback control method refers to CMIS.

Byte	Bits	Field Name	Field Description
13h:128	6	Simultaneous Host And Media Side loopbacks	0b: not supported
	5	Per Lane Media Side Loopbacks	1b: supported
	4	Per Lane Host Side Loopbacks	1b: supported
	3	Host Side Input Loopback	1b: supported
	2	Host Side Output Loopback	1b: supported
	1	Media Side Input Loopback	1b: supported
	0	Media Side Output Loopback	1b: supported

Digital Diagnostic Monitor Accuracy:

The following characteristics are defined over recommended operating conditions.

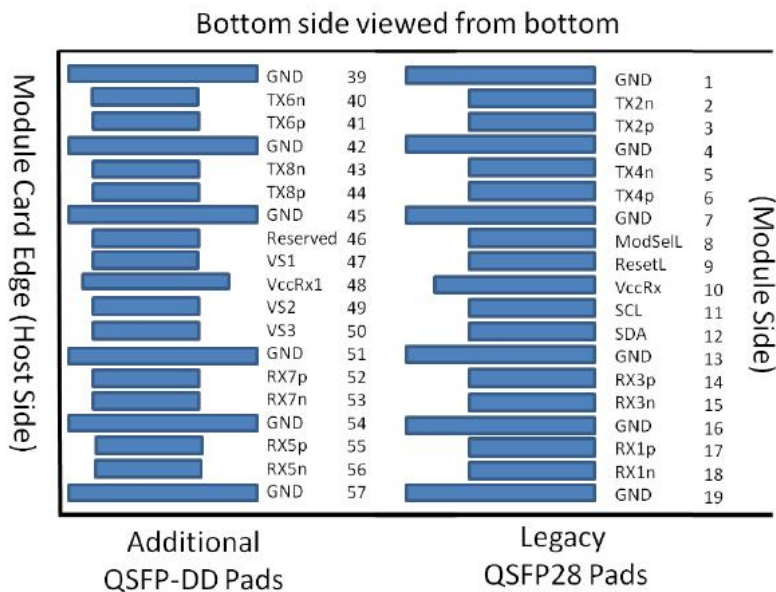
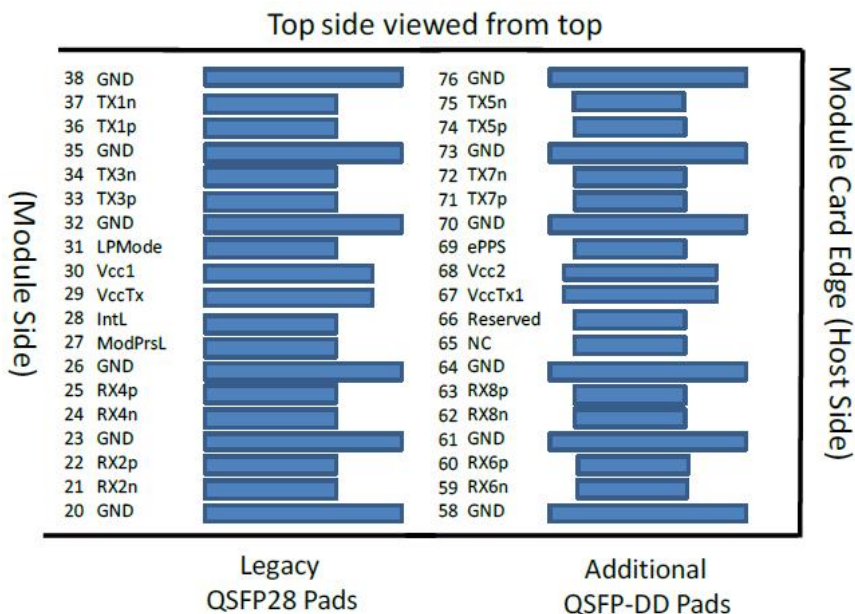
Parameter	Accuracy	Unit
Internally measured transceiver temperature	+/-3	°C
Internally measured transceiver supply voltage	+/-3	%
Measured Tx bias current	+/-10	%
Measured Tx output power	+/-3	dB
Measured Rx received average optical power	+/-3	dB

Notes:

- 1.Test point is the hotspot of the module.
- DDM report stability shall be within 0.5 dB when temperature is stable. TX DDM must report -40 dBm when TX disable.

PIN Definitions:

QSFP-DD Transceiver Pad Layout, host PCB QSFP-DD Pinout, and PIN Descriptions are as follows:



Pin Description:

Pin	Name	Logic	Description	Power Seq	Notes
1	Ground		GND	1B	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	3B	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	3B	
4	Ground		GND	1B	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	3B	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	3B	
7	Ground		GND	1B	1
8	ModSelL	LVTTL-I	Module Select	3B	
9	ResetL	LVTTL-I	Module Reset	3B	
10	VccRx		+3.3V Power Supply Receiver	2B	2
11	SCL	LVC MOS - I/O	2-wire serial interface clock	3B	
12	SDA	LVC MOS - I/O	2-wire serial interface data	3B	
13	Ground		GND	1B	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	3B	
15	Rx3n	CML-O	Receiver Inverted Data Output	3B	
16	Ground		GND	1B	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	3B	
18	Rx1n	CML-O	Receiver Inverted Data Output	3B	
19	Ground		GND	1B	1
20	Ground		GND	1B	1
21	Rx2n	CML-O	Receiver Inverted Data Output	3B	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	3B	
23	Ground		GND	1B	1
24	Rx4n	CML-O	Receiver Inverted Data Output	3B	
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	3B	
26	Ground		GND	1B	1
27	ModPrsL	LVTTL-O	Module Present	3B	

28	IntL	LVTTL-O	Interrupt	3B	
29	VccTx		+3.3V Power supply transmitter	2B	2
30	Vcc1		+3.3V Power supply	2B	2
31	LPMode	LVTTL-I	Low Power mode	3B	
32	Ground		GND	1B	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	3B	
34	Tx3n	CML-I	Transmitter Inverted Data Input	3B	
35	Ground		GND	1B	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	3B	
37	Tx1n	CML-I	Transmitter Inverted Data Input	3B	
38	Ground		GND	1B	1
39	Ground		GND	1A	1
40	Tx6n	CML-I	Transmitter Inverted Data Input	3A	
41	Tx6p	CML-I	Transmitter Non-Inverted Data Output	3A	
42	Ground		GND	1A	1
43	Tx8n	CML-I	Transmitter Inverted Data Input	3A	
44	Tx8p	CML-I	Transmitter Non-Inverted Data Output	3A	
45	Ground		GND	1A	1
46	Reserved		For future use	3A	3
47	VS1		Module Vendor Specific1	3A	3
48	VccRx1		3.3V Power Supply	2A	2
49	VS2		Module Vendor Specific2	3A	3
50	VS3		Module Vendor Specific3	3A	3
51	Ground		GND	1A	1
52	Rx7p	CML-O	Receiver Non-Inverted Data Output	3A	
53	Rx7n	CML-O	Receiver Inverted Data Output	3A	
54	Ground		GND	1A	1
55	Rx5p	CML-O	Receiver Non-Inverted Data Output	3A	
56	Rx5n	CML-O	Receiver Inverted Data Output	3A	
57	Ground		GND	1A	1
58	Ground		GND	1A	1

59	Rx6n	CML-O	Receiver Inverted Data Output	3A	
60	Rx6p	CML-O	Receiver Non-Inverted Data Output	3A	
61	Ground		GND	1A	1
62	Rx8n	CML-O	Receiver Inverted Data Output	3A	
63	Rx8p	CML-O	Receiver Non-Inverted Data Output	3A	
64	Ground		GND	1A	1
65	NC		No Connect	3A	3
66	Reserved		For future use	3A	3
67	VccTx1		3.3V Power Supply	2A	2
68	Vcc2		3.3V Power Supply	2A	2
69	ePPS	LVTTTL-I	Precision Time Protocol (PTP) reference clock input	3A	3
70	Ground		GND	1A	1
71	Tx7p	CML-I	Transmitter Non-Inverted Data Output	3A	
72	Tx7n	CML-I	Transmitter Inverted Data Output	3A	
73	Ground		GND	1A	1
74	Tx5p	CML-I	Transmitter Non-Inverted Data Output	3A	
75	Tx5n	CML-I	Transmitter Inverted Data Output	3A	
76	Ground		GND	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and reserved pads shall have an impedance to GND that is greater than 10Kohms and less than 100pF.

Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

Mechanical Dimensions:

Package dimensions

the package dimensions of the module. 400G LR4 transceivers are compatible with the QSFP-DD Type 2 Specification for pluggable form factor modules.

